

# MC100EPT26

## 1:2 Fanout Differential LVPECL to LVTTTL Translator

The MC100EPT26 is a 1:2 Fanout Differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The VBB output allows the EPT26 to be used in a single-ended input mode. In this mode the VBB output is tied to the  $\overline{D0}$  input for a non-inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01 $\mu$ F capacitor.

- 1.4ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo-random)
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flowthrough Pinouts
- ESD Protection: >2KV HBM, >100V MM
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on  $\overline{D}$
- Q Outputs will default LOW with inputs open or at  $V_{EE}$
- $V_{BB}$  Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.  
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 117 devices

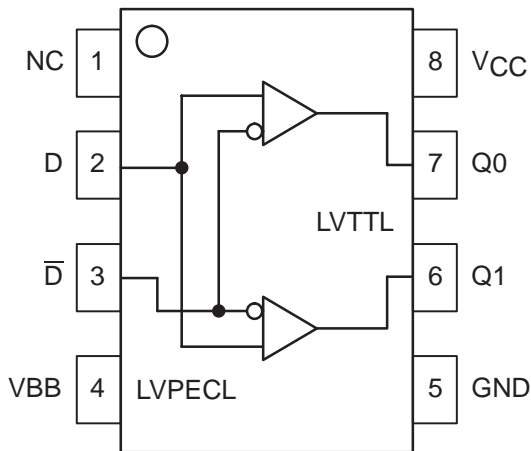
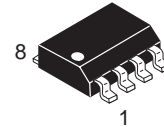


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

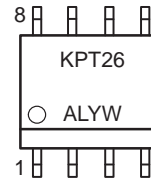


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SO-8  
D SUFFIX  
CASE 751

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D, $\overline{D}$	Differential LVPECL Input Pair
VCC	Positive Supply
VBB	Reference Voltage
GND	Ground

### ORDERING INFORMATION

Device	Package	Shipping
MC100EPT26D	SOIC	98 Units/Rail
MC100EPT26DR2	SOIC	2500 Tape & Reel

# MC100EPT26

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply (GND = 0V)	0 to 3.8	VDC
$V_I$	Input Voltage (GND = 0V, $V_I$ not more positive than $V_{CC}$ )	0 to 3.8	VDC
$I_{out}$	Output Current Continuous Surge	50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source Current†	± 0.5	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
$T_{sol}$	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

## DC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ; GND = 0V; $T_A = -40^\circ C$ to $85^\circ C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CCH}$	Power Supply Current (Outputs set to HIGH)	10	20	18	mA
$I_{CCL}$	Power Supply Current (Outputs set to LOW)	15	28	35	mA
$V_{IH}$	Input HIGH Voltage ( $V_{CC} = 3.3$ ) (Note 1.)	2135		2420	mV
$V_{IL}$	Input LOW Voltage ( $V_{CC} = 3.3$ ) (Note 1.)	1490		1825	mV
$I_{IH}$	Input HIGH Current			150	μA
$I_{IL}$	Input LOW Current	$\frac{D}{D}$ -150		0.5	μA
$V_{OH}$	Output HIGH Voltage ( $I_{OH} = -3.0mA$ ) (Note 2.)	2.4			V
$V_{OL}$	Output LOW Voltage ( $I_{OL} = 24mA$ ) (Note 2.)			0.5	V
$I_{OS}$	Output Short Circuit Current	-50		-150	mA
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V
$V_{BB}$	Output Voltage Reference		2.0		V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with  $V_{CC}$ .
2. All loading with 500 ohms to GND,  $CL = 20pF$ .
3.  $V_{IHCMR}$  min varies 1:1 with GND, max varies 1:1 with  $V_{CC}$ .

## AC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ; GND = 0V)

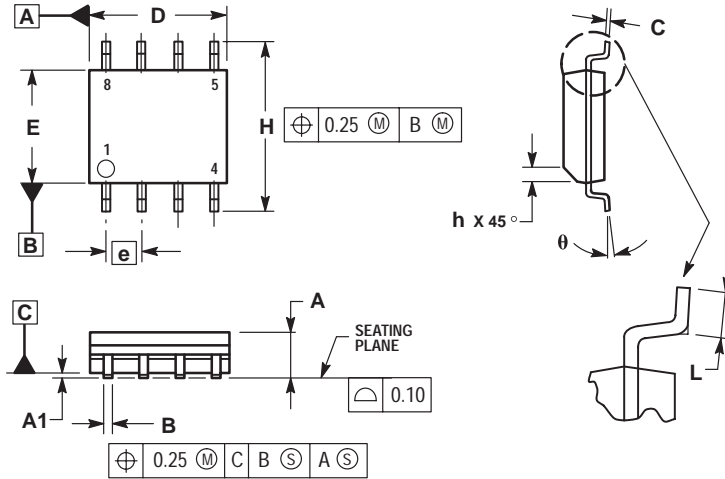
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency (Note 4.)	275			275			275			MHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	500	1500	2500	500	1500	2500	500	1500	2500	ps
$t_{SK+ +}$ $t_{SK- -}$ $t_{SKPP}$	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% – 80%) $Q, \bar{Q}$	330	500	900	330	500	900	330	550	950	ps

4.  $f_{max}$  guaranteed for functionality only.  $V_{OL}$  and  $V_{OH}$  levels are guaranteed at DC only.
5. Skews are measured between outputs under identical transitions.

# MC100EPT26

## PACKAGE DIMENSIONS


SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-06  
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
$\theta$	0°	7°

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